

A SINGLE-BURST-CORRECTION / DOUBLE-BURST-DETECTION ERROR CODE

ABSTRACT

A method and apparatus for performing encoding and decoding
5 of bit chain data packets conveying errors which do not spread on
more than n bits, at very high speed are here disclosed. The
matrix of the corresponding Systematic code is built using $p \times p$
matrix blocks comprising elements of the galois field GF ,
generated by an irreducible generator polynomial of degree p , p
10 being greater or equal to n . With the preferred embodiment of the
invention, the decoding operation includes an error detection
which distinguishes errors between correctable and non
correctable errors. The errors limited inside fixed size bursts
are 100% corrected if confined to one burst and are all detected
15 if spread on two bursts. The ASIC implementation of the decoding
method of the invention requires only a combinatorial logic. The
method and apparatus of the invention allows a 21 bit error code
applied to a typical 512 bit data packets transported on 8B/10B
coded 2.5 Gbps serial links to be moved at a speed in the range
20 of Tbps in a telecommunications equipment with the level of
correction and detection mentioned above.